IN THE CLAIMS

Please amend the claims as follows:

Claims 1-4 (Canceled).

Claim 5 (Currently Amended): A semiconductor device including a trench gate IGBT, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type which is formed on one surface of said first semiconductor layer;

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer;

emitter layers of the second conductivity type which are selectively formed in a surface portion of said base layer;

a plurality of trenches which extend through said emitter layers and said base layer and are formed to a predetermined depth in the second semiconductor layer;

gate electrodes which are formed on gate insulating films in the trenches;

an emitter electrode which is formed on said emitter layers and said base layer;

a collector electrode which is formed on the other surface of said first semiconductor layer;

an auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches and is insulated from said emitter electrode; and

a carrier discharge electrode which contacts a surface of said auxiliary base layer of the first conductivity type;

further comprising a MISFET including a channel region of the first conductivity type;

wherein a source of said MISFET is connected to said carrier discharge electrode of the trench gate IGBT, and a drain of said MISFET is connected to said emitter electrode of the trench gate IGBT;

wherein said MISFET is mounted in the same package as a package of the trench gate IGBT;

~~A device according to claim 4,~~ wherein said MISFET is formed on a third semiconductor layer which is formed on said second semiconductor layer and insulated from said second semiconductor layer.

Claim 6 (Currently Amended): A semiconductor device including a trench gate IGBT, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type which is formed on one surface of said first semiconductor layer;

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer;

emitter layers of the second conductivity type which are selectively formed in a surface portion of said base layer;

a plurality of trenches which extend through said emitter layers and said base layer and are formed to a predetermined depth in the second semiconductor layer;

gate electrodes which are formed on gate insulating films in the trenches;

an emitter electrode which is formed on said emitter layers and said base layer;

a collector electrode which is formed on the other surface of said first semiconductor layer;

an auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches and is insulated from said emitter electrode; and

a carrier discharge electrode which contacts a surface of said auxiliary base layer of the first conductivity type;

further comprising a MISFET including a channel region of the first conductivity type;

wherein a source of said MISFET is connected to said carrier discharge electrode of the trench gate IGBT, and a drain of said MISFET is connected to said emitter electrode of the trench gate IGBT;

wherein said MISFET is mounted in the same package as a package of the trench gate IGBT;

~~A device according to claim 4,~~ wherein said MISFET is mounted on a frame different from a frame of the trench gate IGBT.

Claim 7 (Original): A device according to claim 6, wherein said MISFET includes a vertical MISFET in which a source and a drain are vertically positioned.

Claim 8 (Currently Amended): A semiconductor device including a trench gate IGBT, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type which is formed on one surface of said first semiconductor layer;

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer;

emitter layers of the second conductivity type which are selectively formed in a surface portion of said base layer;

a plurality of trenches which extend through said emitter layers and said base layer and are formed to a predetermined depth in the second semiconductor layer;

gate electrodes which are formed on gate insulating films in the trenches;

an emitter electrode which is formed on said emitter layers and said base layer;

a collector electrode which is formed on the other surface of said first semiconductor layer;

an auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches and is insulated from said emitter electrode; and

a carrier discharge electrode which contacts a surface of said auxiliary base layer of the first conductivity type;

further comprising a MISFET including a channel region of the first conductivity type;

wherein a source of said MISFET is connected to said carrier discharge electrode of the trench gate IGBT, and a drain of said MISFET is connected to said emitter electrode of the trench gate IGBT;

~~A device according to claim 2~~ wherein said MISFET and the trench gate IGBT are mounted in different packages.

Claim 9 (Original): A device according to claim 8, wherein the trench gate IGBT comprises a first comb electrode connected to said emitter electrode, and a second comb

electrode which faces the first comb electrode and is connected to said carrier discharge electrode.

Claim 10 (Original):A device according to claim 8, wherein the trench gate IGBT comprises a first interconnection layer connected to said carrier discharge electrode, and a second interconnection layer connected to said emitter electrode, and the first interconnection layer and the second interconnection layer are vertically so arranged as to sandwich an insulating film.

Claim 11 (Original): A semiconductor device including a trench gate IGBT, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type which is formed on one surface of said first semiconductor layer;

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer;

emitter layers of the second conductivity type which are selectively formed in a surface portion of said base layer;

a plurality of trenches which extend through said emitter layers and said base layer and are formed to a predetermined depth in the second semiconductor layer;

gate electrodes which are formed on gate insulating films in the trenches;

an emitter electrode which is formed on said emitter layers and said base layer;

a collector electrode which is formed on the other surface of said first semiconductor layer;

a first auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches and is insulated from said emitter electrode;

a second auxiliary base layer of the second conductivity type which is formed on the first auxiliary base layer of the first conductivity type in the region;

a third auxiliary base layer of the first conductivity type which is formed on the second auxiliary base layer of the second conductivity type in the region and contacts said emitter electrode; and

a carrier discharge electrode which contacts a surface of said third auxiliary base layer of the first conductivity type.

Claim 12 (Original): A device according to claim 11, further comprising:

at least one auxiliary trench which is so formed as to extend through said third auxiliary base layer of the first conductivity type and said second auxiliary base layer of the second conductivity type and reach a predetermined depth in said third auxiliary base layer of the first conductivity type in the region where said first auxiliary base layer of the first conductivity type, said second auxiliary base layer of the second conductivity type, and said third auxiliary base layer of the first conductivity type are formed; and

an auxiliary gate electrode which is formed on a gate insulating film in the auxiliary trench.

Claim 13 (Canceled).

Claim 14 (Canceled).

Claim 15 (Currently Amended): A semiconductor device including a trench gate IGBT, comprising:

a trench gate IGBT having

a first semiconductor layer of a first conductivity type,

a second semiconductor layer of a second conductivity type which is formed on one surface of the first semiconductor layer,

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer,

emitter layers of the second conductivity type which are selectively formed in a surface portion of the base layer,

a plurality of trenches which extend through the emitter layers and the base layer and are formed to a predetermined depth in the second semiconductor layer,

gate electrodes which are formed on gate insulating films in the trenches,

an emitter electrode which is formed on the emitter layers and the base layer,

a collector electrode which is formed on the other surface of the first semiconductor layer,

an auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches, and

a carrier discharge electrode which contacts a surface of the auxiliary base layer of the first conductivity type; and

a MISFET which includes a channel region of the first conductivity type, and includes a source connected to the carrier discharge electrode of the trench gate IGBT, a drain connected to the emitter electrode of the trench gate IGBT, and a gate electrode electrically connected to the gate electrode of the trench gate IGBT;

wherein said MISFET is mounted in the same package as a package of the trench gate IGBT;

~~A device according to claim 14,~~ wherein said MISFET is formed on a third semiconductor layer which is formed on said second semiconductor layer and insulated from said second semiconductor layer.

Claim 16 (Currently Amended): A semiconductor device including a trench gate IGBT, comprising:

a trench gate IGBT having

a first semiconductor layer of a first conductivity type,

a second semiconductor layer of a second conductivity type which is formed on one surface of the first semiconductor layer,

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer,

emitter layers of the second conductivity type which are selectively formed in a surface portion of the base layer,

a plurality of trenches which extend through the emitter layers and the base layer and are formed to a predetermined depth in the second semiconductor layer,

gate electrodes which are formed on gate insulating films in the trenches,

an emitter electrode which is formed on the emitter layers and the base layer,

a collector electrode which is formed on the other surface of the first semiconductor layer,

an auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches, and

a carrier discharge electrode which contacts a surface of the auxiliary base layer of the first conductivity type; and

a MISFET which includes a channel region of the first conductivity type, and includes a source connected to the carrier discharge electrode of the trench gate IGBT, a drain connected to the emitter electrode of the trench gate IGBT, and a gate electrode electrically connected to the gate electrode of the trench gate IGBT;

wherein said MISFET is mounted in the same package as a package of the trench gate IGBT;

~~A device according to claim 14,~~ wherein said MISFET is mounted on a frame different from a frame of the trench gate IGBT.

Claim 17 (Original): A device according to claim 16, wherein said MISFET includes a vertical MISFET in which a source and a drain are vertically positioned.

Claim 18 (Currently Amended): A semiconductor device including a trench gate IGBT, comprising:

a trench gate IGBT having

a first semiconductor layer of a first conductivity type,

a second semiconductor layer of a second conductivity type which is formed on one surface of the first semiconductor layer,

a base layer of the first conductivity type which is formed in a surface portion of the second semiconductor layer,

emitter layers of the second conductivity type which are selectively formed in a surface portion of the base layer,

a plurality of trenches which extend through the emitter layers and the base layer and are formed to a predetermined depth in the second semiconductor layer,

gate electrodes which are formed on gate insulating films in the trenches,

an emitter electrode which is formed on the emitter layers and the base layer,

a collector electrode which is formed on the other surface of the first semiconductor layer,

an auxiliary base layer of the first conductivity type which is formed in an arbitrary region between two adjacent trenches, and

a carrier discharge electrode which contacts a surface of the auxiliary base layer of the first conductivity type; and

a MISFET which includes a channel region of the first conductivity type, and includes a source connected to the carrier discharge electrode of the trench gate IGBT, a drain connected to the emitter electrode of the trench gate IGBT, and a gate electrode electrically connected to the gate electrode of the trench gate IGBT;

~~A device according to claim 13,~~ wherein said MISFET and the trench gate IGBT are mounted in different packages.

Claim 19 (Original): A device according to claim 18, wherein the trench gate IGBT comprises a first comb electrode connected to said emitter electrode, and a second comb electrode which faces the first comb electrode and is connected to said carrier discharge electrode.